Readout Technology for > 1K x 1K Staring Focal Plane Arrays

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ABSTRACT

Until recently, very large focal plane arrays (> 1K x 1K pixels) could only be fabricated using low density ≥ 2 μm CMOS processes employing full wafer projection lithography. Higher density processes use steppers to expose the patterns on the wafer which have limited the die size to the area able to be exposed in a single step. This placed an upper limit on the readout die size of about 18-22 mm along a side. While stitching techniques have been used to pattern larger die, most silicon foundries are unwilling to accept such projects. Raytheon has recently pioneered a foundry friendly technique that allows an arbitrarily large readout to be fabricated using advanced submicron (0.6 to 0.8 μm) and deep submicron (0.25 to 0.35 μm) CMOS processes.

In July 1998, Raytheon fabricated a 2052 x 2052 readout with 25 μm x 25 μm pixels for a low background astronomy application. This readout was 54.7 mm x 54.7 mm in size - more than 4x the area of the 22 mm x 22 mm mask size. In 1999, Raytheon will produce two different tactical imaging FPAs in > 1K x 1K formats using pixel sizes ranging from 20-25 μm. These tactical FPAs will be processed in a triple metal, 0.5 μm CMOS process and range in size from 23 mm x 23 mm to nearly 40 mm x 40 mm. InSb FPAs using these readout integrated circuits (ROIC) will be fabricated this year.

Introduction

At the dawn of the new millennium, megapixel IRFPAs are becoming a reality. The progression of 2nd generation staring array pixel count has roughly tracked the growth in DRAM array sizes since the early 1980's. Staring array size progression is summarized in Figure 1 which compares the growth of pixel count over time for a variety of detector technologies with the exponential increase in production DRAM bits per chip. DRAM development and production has fueled the drive to achieve ever finer lithography resolution while increasing wafer size to survive in the fiercely competitive market for computer memory chips. IRFPAs, particularly staring arrays, rely on the progression of silicon integrated circuit processing technology to achieve the array size increases and pixel size reductions desired for larger formats. Focal plane pixel count lags DRAM growth for three main reasons. First, DRAM technology requires only on transistor per bit, while focal plane readouts require a minimum of two (for the simple DI - more complex circuits need 3 - 6 or more transistors per input). Second, DRAM circuits are digital devices and store only a single bit of information per memory element, while FPAs are analog devices and store 12-14 bits of information in each pixel. Third, the market for focal planes is a tiny fraction of that for computer memory and the foundries available for readout fabrication are typically one or two upgrades behind those used by the state of the art DRAM production.

Large staring focal plane evolution has been driven by astronomy applications. While this is somewhat surprising given the comparative budget sizes of the defense market and the astronomical community, astronomers have funded

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large focal plane development to dramatically improve telescope throughput. The 1kx1k Aladdin IRFPA can capture 16 times the sky area of a 256 x 256 array in a single exposure![1]

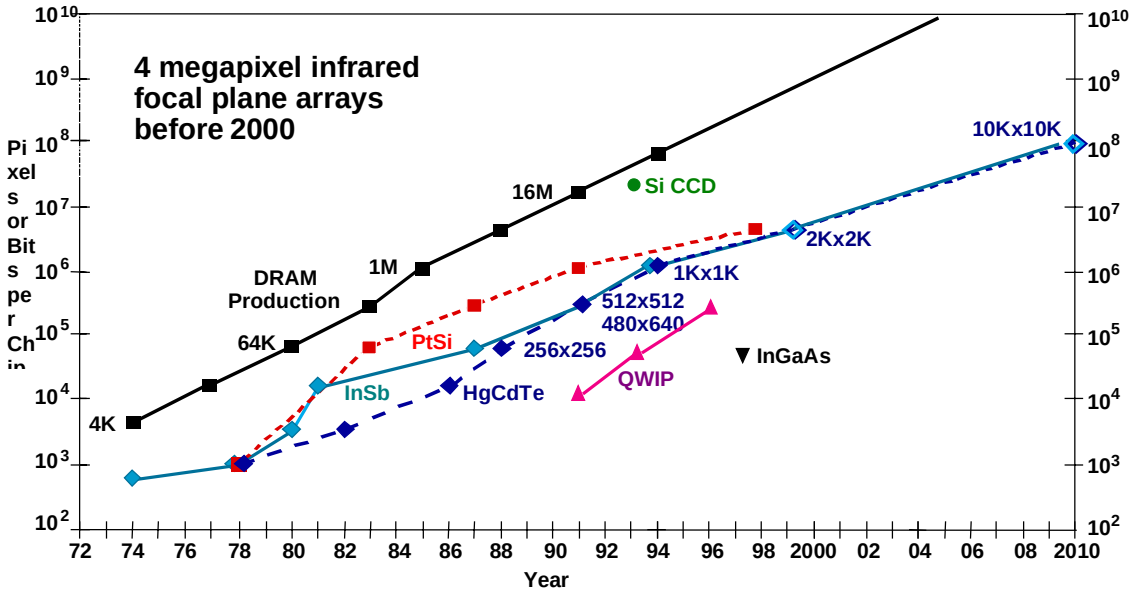

Figure 1 Progress in infrared staring focal plane array pixel count for a variety of detector materials compared with the exponential increase in DRAM bits per chip since 1972.

Previous Readout Array Size Limitations

Until recently, two primary factors have limited the die size of staring FPA readouts: photolithography tools and process defect density. Photolithography tooling is needed to expose the circuit patterns on the silicon wafers during processing. Three primary types of lithography tools have been used: 1x Projection Aligners, 1x Reticle Wafer Steppers, and 5x Reticle Wafer Steppers. 1x aligners (P&E, SVGL) use large glass plates to expose the entire surface of the wafer in one operation allowing a circuit to cover the entire wafer if desired. However, to the large optical field of view and lack of magnification limits the size of CMOS features to ≥ 2 μm. Only relatively simple detector input circuits such as a DI (Direct Injection) or SFD (Source Follower per Detector) can be processed in the small 20-30 μm unit cells needed for IRFPAs larger than 256 x 256. The 1K x 1K arrays, which have been produced for astronomical observatories since 1994 used this technique with the simple SFD input circuit.

In the late 80's, 1x Reticle Wafer Steppers (Ultratech) were employed to resolve features down to about 1 - 1.2 μm. However, the maximum square die size was 14.1 x 14.1 mm. This die size limitation proved adequate for 640 x 480 readouts but was clearly too small for anything larger. Even some complex 640 x 480 or 512 x 512 format arrays were forced to stitch two aligner fields together to pattern a full die. The yield of these stitched arrays was usually quite poor, required multiple sets of reticles (1 for each piece of the device), and significantly reduced the wafer throughput of the wafer steppers. "stitching" or multiple reticle composition is expensive in terms of the additional three reticles required for each of a dozen mask layers and in some implementations, special lithography equipment. Also, at the silicon foundry, handling multiple reticles impedes the factory's workflow and capital equipment utilization.

5x Reticle Wafer Steppers (ASML, Nikon, Canon) were introduced for advanced submicron (0.5 to 0.8 μm) and deep submicron (≤ 0.35 μm) CMOS processes. The reticle image apertures of these aligners, while larger than the previous 1x steppers, still limits the die size to 18 to 22 mm.

In addition to the lithographic die size limit, the CMOS process defect density in most if not all 1-2 μm fabs is too high to achieve acceptable yields for production of large staring (≥1k x 1k) readouts needed for terrestrial (rather than celestial) imaging. Yield improvements of 5-10x have been routinely achieved when older designs have been ported to state-of-the-art analog or mixed signal CMOS processes in a 6 or 8" fab.

Large Staring Die Sizes Will Increase Dramatically

As the IRFPA array sizes increase to improve field of view coverage and/or resolution, pixel sizes are not going to be significantly reduced below the 17-20 μm typical of today's 640 x 480 arrays - unlike the size of a DRAM memory cell which has been steadily reduced. While there will be some reduction, mainly for medium- and short-wavelength detectors, optical diffraction will limit these reductions. The size of a diffraction-limited optical spot of Airy disk is given by:

$$d = 2.44 \lambda f$$

where d is the diameter of the spot, λ is the wavelength, and f is the f-number of the focusing lens. The spot size for f-numbers ranging from f/1 to f/10 are shown in Figure 2 for the typical IR wavelengths. Currently production MWIR FPAs - in 480 x 640 formats - have 20 μm pixels. System users typically prefer some degree of oversampling and therefore, pixel size may eventually be reduced for MWIR application to about 10-12 μm - giving a 4x oversample. In principle, LWIR pixel sizes should not be reduced much below 20 μm (for f/2 systems). However, since most tactical readouts are used for both MWIR and LWIR applications, the LWIR pixel size will likely be reduced as well. The smallest IRFPA pixels will likely be found in specialized SWIR applications demanding maximum spatial resolution.[2]

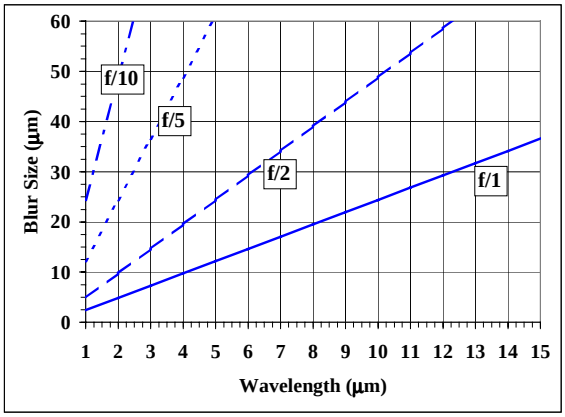

Figure 2 – Optics Diffraction Limt. The spot size of a diffraction limited optical system is the Airy disk diameter.

Raytheon Pioneers New Lithography Technique

In a July 19, 1999 press release, AMI (American Microsystems Inc.) announced a new lithography technique that allows the fabrication of huge, seamless CMOS imaging arrays.[3] The lithography technique, called Reticle Image Composition Lithography (RICL), was conceived at Raytheon in 1997 and has since been used to design and fabricate several megapixel IRFPAs. The Megapixel or Ultra Large Scale (ULS) readout arrays designed using the technique are shown in Table I. For comparison, the table also lists the conventionally fabricated 640 x 512 readout as well as some comparable state-of-the-art microprocessors from Intel Corporation.[4]

Table I – Megapixel Readout Arrays Under Development at Raytheon. The readouts using the RICL technique are indicated in bold face type.

Array Format	# of Pixels	Die Size (mm)	# of Transistors	Process Technology
640 x 512	3.3×10^3		$\sim 2.3 \times 10^6$	0.8 μm 2poly/2metal
1,024 x 1,024	**1.0×10^6**	**22 x 28**	**$\sim 2.5 \times 10^6$**	**0.5 μm 2 poly/3 metal**
1,344 x 1,344	**1.8×10^6**	**37 x 39**	**$\sim 4.0 \times 10^6$**	**0.5 μm 2 poly/3 metal**
2,052 x 2,052	**4.2×10^6**	**54 x 54**	**$\sim 30 \times 10^6$**	**0.6 μm 2 poly/2 metal**
Pentium® III	N/A		9.5×10^6	0.25 μm
Celeron™	N/A	31 x 35	19×10^6	0.25 to 0.18 μm

The RICL concept can be applied successfully to the class of integrated circuit architectures that are naturally repetitive; infrared readouts are generally well within this class. Consider the standard two-dimensional IR imager floorplan, see Figure 3, with an arrayed core of input circuits in the center with multiplexing circuits and digital sequencing logic around the sides and other overhead in the corners. If a "tick-tack-toe" grid is placed over the ROIC floorplan along the edge of the input circuit array, then the readout is divided into nine sections. Each section of the design is designated with a two-character mnemonic; AA for the input circuit array, C1-4 for the corners, HT and HB for the horizontal top and bottom and VL and VR for the vertical left and right. Making larger devices then is simply at matter of repeating the five central circuit sections AA, HT, HB, VL and VR.

However, RICL requires that image areas be free of alignment targets and that reticle images have good registration. The technological enabler for this requirement appeared at AMI in 1991 embodied in its first ASM Lithography 5500/60 5x wafer stepper. This machine and its successors, the model 5500/200s in AMI's Fab10, have only two alignment targets on the entire 200 mm wafer. No targets are required in the product images on any reticle. The second and key feature of these ASML 5x systems is that their registration of any printed image on the wafer is 0.10 μm or better. With these two features of the ASM steppers, ROIC reticle images can be registered and overlaid with no intervention on the part of the foundry production staff.

Figure 4 shows a completed RICL project built in July 1998. This ROIC was formed by a 3 x 3 matrix of the core AA cell and three each of the two horizontal and vertical segments. The smaller die in the corners of the wafer are the small test die which exceed the size of a contemporary 640 x 480 readout. For configuration control these test die are now referred to as *chipname*[xy] where the xy is the X-Y count of the number of AA type reticle images for that readout. The five product die, *chipname*[CC], are 55 mm squared and have over 30 million transistors. The chipname and the brackets are patterned in the top-level CMOS metal mask and the AA image X-Y count is patterned by Raytheon using an indium interconnect mask or by other means.

In the readout design environment, RICL-based circuits are broken into the nine sections exhibited in Figure 3 with each section represented as a separate schematic. Typically, the HT schematic section has the multiplexer and the X-shift register, the VR section contains the Y-shift register, the C4 section may contain bias generators and the C3 schematic contains the ROIC command and controller logic. Strict use of the RICL section schematics has a number of benefits. Each schematic section can be LVS'd and DRC'd as a separate circuit. Larger variants in the array size of a RICL-based ROIC design can be created by a new schematic that interconnects the nine RICL circuit sections and additional vertical, horizontal and array sections in one or both axes as appropriate. These very large-scale readouts can be easily simulated, and with the corresponding layouts, they can verified by LVS and DRC runs.

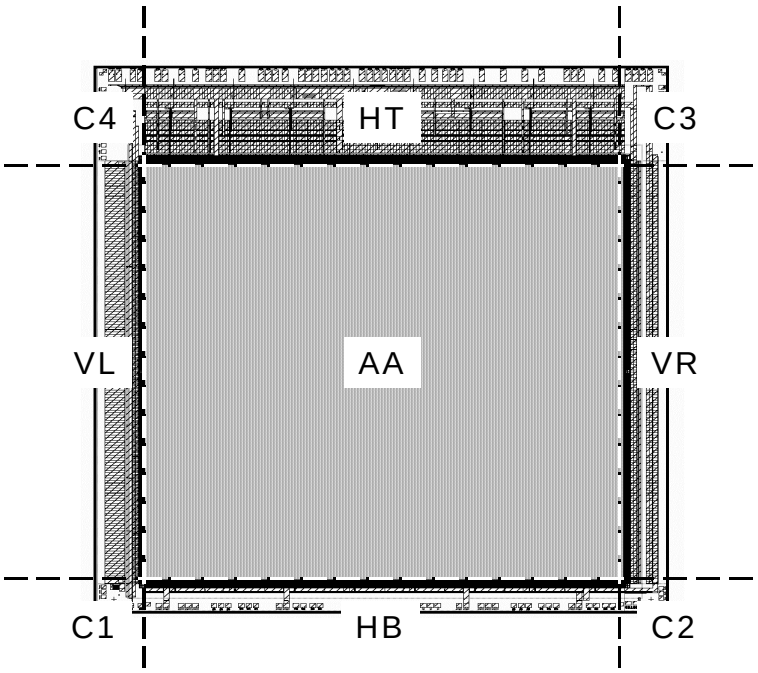

Figure 3 – Typical RICL-based ROIC Design with Sections Designated

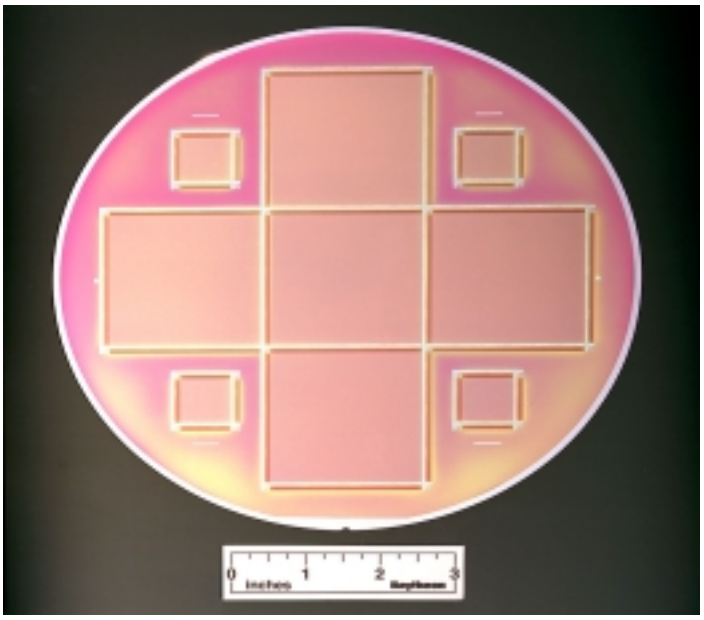

Figure 4 – 2,052 x 2052 readouts for astronomy applications have been produced.

Megapixel Readouts Require Advance Circuit Techniques

Megapixel readouts present unique challenges to the IC designer. The arrays still need to be cryogenically cooled. The larger die sizes create a larger static heat load since the dewar platform and coldshield must be increased in size as well. The active power dissipation of these arrays clearly cannot scale upward as well with current and projected

stirling cooler capacities. Active power management must be employed to deliver power to thirsty analog circuitry only when required. The submicron processes used for advanced megapixel readouts also operate with reduced voltages (3.3 to 5 V versus 6 to 10 V previously). The lower voltage rails have driven designers to make extensive use of differential op amps to maximize output voltage swings. The days of a chain of source followers are likely gone.

Also, near 100% duty cycle multiplexer design is required to reduce row and frame setup latencies. A 1 μsec row setup time adds over 1 msec to the read time of a 1K array while producing no active data at the output. High speed, low power output drivers must be employed to achieve the >30 Hz frame rates desired for these huge arrays. Raytheon has developed differential current mode output drivers capable of operating at >10 MHz while dissipating only 2mW per pair of outputs. This is more than a 5x improvement over the equivalent voltage mode output. External differential receivers have also been developed to buffer the output current into an A/D converter in the system electronics.

The large optical focal plane of these devices also creates another challenging problem. Most systems using these large arrays require relatively short cold shields (1-2") which create a severe rolloff in illumination near the edges and corners of these arrays (see Figure 5). To preserve the system dynamic range Cos^4 optical shading correction has been done to apply higher on-chip gain for pixels away from the optical axis.

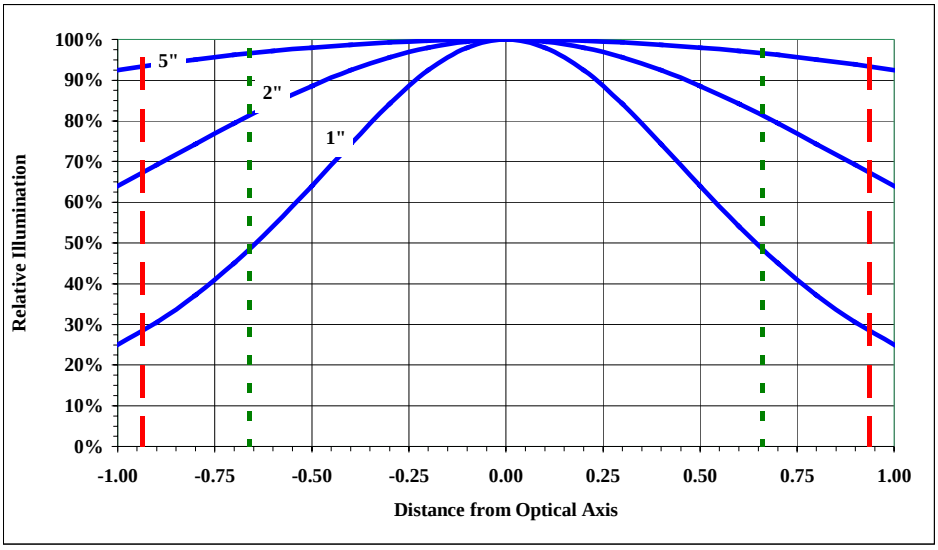

Figure 5 – Cos^4 off-axis optical shading causes severe gain loss near the sides and corners of a 1344 x 1344 array. Optical shading for three different cold shield lengths (1", 2", and 5") are plotted. vertical dashed lines in the figure show the distance to the sides and corners of the FPA. On-chip gain compensation can reduce or eliminate this effect.

Finally, the IC designs must be made tolerant to process variations and process defects. Programmable process adjust circuitry has been developed to allow the chips to compensate for process variations. Also, process tracking reference sources are included where possible and practical. The large die area increases the likelihood that defects will fall in a die – even with the reduced process defect density typical of the class 1 cleanroom facilities used to fabricate these devices. Particular care is given to the unit cells (detector input circuit) which represent over 90% of the die area. In several of Raytheon's designs, over 70% of the unit cell area is filled with an integration capacitor. Raytheon's circuits are designed to isolate these defects to the single unit cell with the shorted capacitor.

Large Staring Products are in Design and Fabrication

As mentioned above, several large staring FPAs are being designed and fabricated at Raytheon in 1998 and 1999. The first large staring readout designed and produced was a 2,052 x 2,052 array for very low background astronomy applications (see Figure 4). FPAs have yet to be made from these arrays. The second device was designed as a large staring demonstration device suitable for terrestrial or tactical imaging. The initial data from one of these devices, while preliminary, looks very encouraging. The first lot of SB-199[BB] readouts (a 1344 x 1344 array with 25 μm pixels) has been completed and is in evaluation (see Figure 6). All wafers contained several functional readouts though final yield numbers have yet to be determined. A few prototype InSb FPAs have also been fabricated (see Figure 7) from this initial lot. These FPAs are the largest InSb devices ever made. It should be noted that this work has been done using the same equipment as the high rate production programs here at the Raytheon Infrared Center of Excellence.

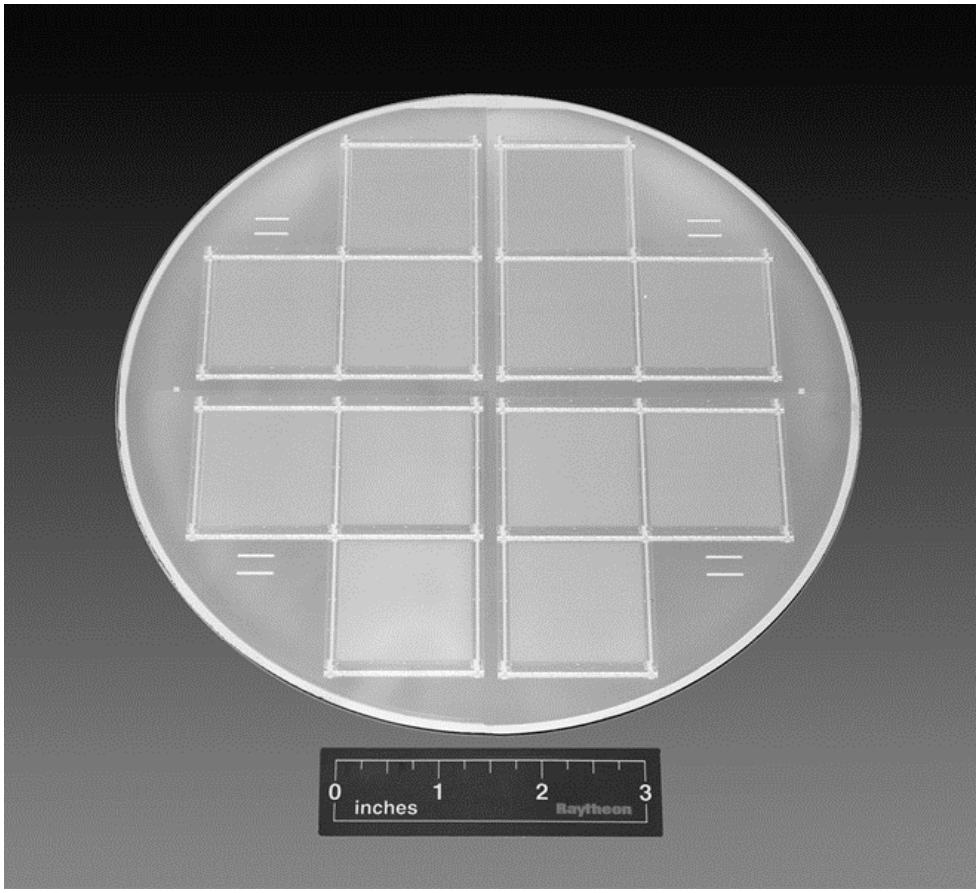

Figure 6 – 1344 x 1344 RICL Readout Wafer. Twelve 1344 x 1344 readouts are processed on each 8" wafer.

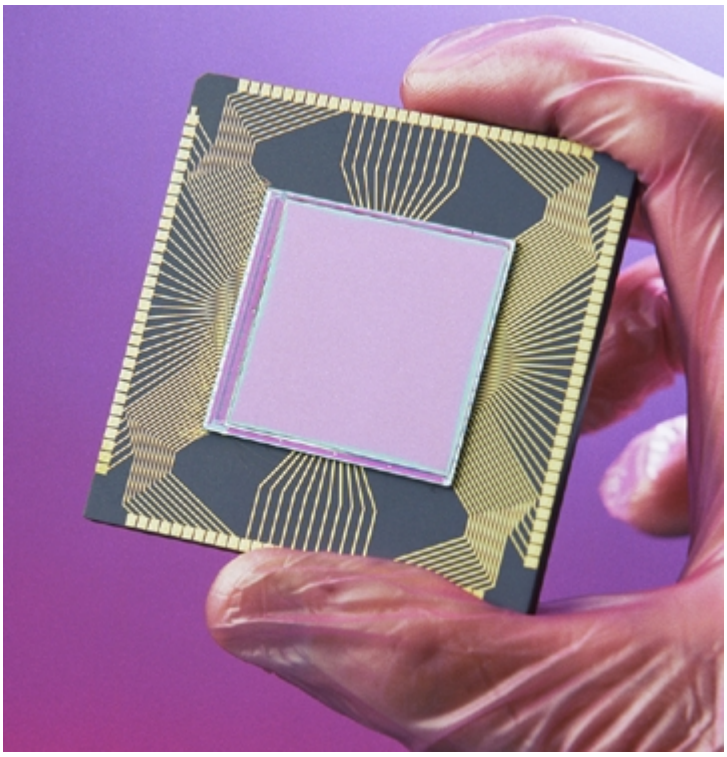

Figure 7 – Worlds largest InSb FPA is mounted on a custom 124 pin leadless chip carrier ready for test. The FPA contains over 1.8 million pixels.

Summary

Raytheon has pioneered a new foundry friendly photolithography technique called Reticle Image Composition Lithography (RICL). RICL allows arbitrarily large readout ICs to be designed using state-of-the-art submicron and deep submicron CMOS processes. Further a single design database and reticle mask set can be used to fabricate a family of N x M format arrays. Two large format staring readout arrays (each larger than the image area of the 5x reticles used) have been fabricated at AMI and a third is in design. Prototype InSb FPAs have been successfully fabricated and are in test and evaluation. Raytheon is leveraging its long history of rate production of smaller 2nd generation FPAs to fabricate these megapixel FPAs using production equipment and tooling.

References

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[4]Intel Corporation, http://www.intel.com/pressroom/kits/processors/quickref.htm. Pentium® III and Celeron™ are registered trademarks of Intel Corporation.